Title: SELECTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO REDUCE TEST TIME

Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 1 of 3

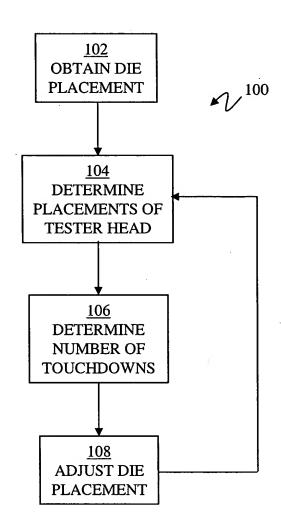


FIG. 1

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Sheet 2 of 3

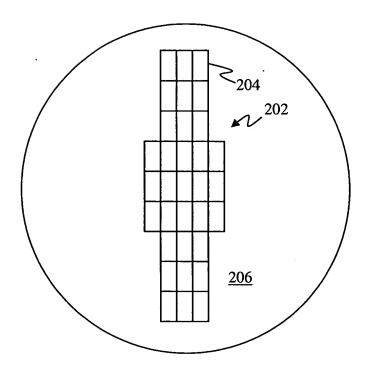


FIG. 2-A

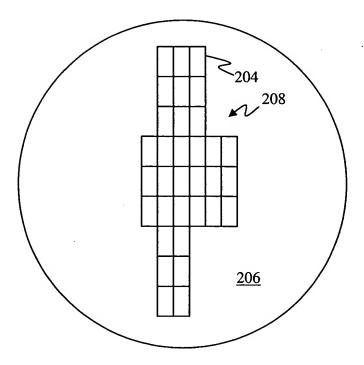


FIG. 2-B

